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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/613,577
Filing Date: July 02, 2003
Appellant(s): YOSHIHARA, KOICHI

Michael A. Nelson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/10/2009 appealing from the Office action mailed 8/27/2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5920220	Takao et al.	7-1999
7031405	Touzni et al.	4-2006
10/617,577*	Yoshihara, Koichi	7-2003

* Where 10/617,577 is the instant application, titled "half-Symbol Constellation display".

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (US 5,920,220) in view of the admitted prior art of the instant application.

- The claim 9 rejection cited in pages 5 of the Non-final office action, dated 12/31/2008, and pages 6 of the Final office action, dated 7/29/2009 as follows-
--- With regard claim 9, which is a method claim related to claim 2, all limitation is contained in claim 2. The explanation of all the limitation is already addressed in the above paragraph. ---

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Since Examiner withdrawn the claim 2 rejection with respect to the 35 USC 112 6th paragraph, Examiner rewrites the detailed claim 9 rejection here below.

With regard claim 9, Takao et al. discloses a method comprising:

deriving quadrature component signals and a symbol clock from the modulated signal (Fig.35 element 5j and column 25 lines 16-35, where examiner considers the t_0 as symbol clock that is generated based on the demodulated IF signal. It is inherent that the IF signal is derived from a modulated signal transmitted by a transmitter.);

generating a sample clock having a period equal to the symbol clock (Fig.35 elements 51 and 52 outputs, t_a and t_b), the sample clock being shifted one-half period in phase with respect to the symbol clock (Fig.35 element 31a, where the $+\delta t$ 52 and $+\delta t$ 51 are predetermined amount of phase shift can be set to any period in phase with respect to t_0 (symbol clock)); and

sampling the quadrature component signals with the sample clock to produce pseudo-symbols as pairs of pseudo-symbols about a symbol sample point for each symbol (Fig.35, outputs of A/D converters, 2 and 3, where the quadrature modulated signals from the outputs of quadrature detector are sampled by the sampling clock output from element 5e to generate the sample pairs, known as pseudo-symbol as defined by the specification of the instant application (page 4 lines 10-13) that are symmetric about a symbol sample point.)

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Takao et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching means for displaying the pseudo-symbols on a quadrature coordinate plane.

However, the admitted prior art of the instant application teaches means for displaying the pseudo-symbols on a quadrature coordinate plane (Fig.5 elements 36 and 38, where Fig.5 without element 30, MOD (delay), is a conventional receiver (page 11, lines 1-16).) in order to display the distortion so that the distortion can be corrected to improve the quality. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include memory 36 and display 38 as taught by the admitted prior art of the instant application into Fig.35 of the Takao's receiver circuitry to receive the output signals of the A/D converters 2 and 3 in order to display the distortion so that the distortion can be corrected to improve the quality.

3. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (US 5,920,220) and the admitted prior art of the instant application as applied to claim 2 above, and further in view of Touzni et al. (US 7,031,405).

- The claim 10 rejection cited in pages 6 of the Non-final office action, dated 12/31/2008, and pages 7 of the Final office action, dated 7/29/2009 as follows.
--- With regard claim 10, which is a method claim related to claim 3, all limitation is contained in claim 3. The explanation of all the limitation is already addressed in the above paragraph. ---

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Since Examiner withdrawn the claim 3 rejection with respect to the 35 USC 112 6th paragraph, Examiner rewrites the detailed claim 9 rejection here below.

With regard claim 10, Takao et al. and the admitted prior art of the instant application disclose all of the subject matter as described in the above paragraph except for specifically teaching means for generating a template for the displaying representing an ideal modulated signal.

However, Touzni et al. teaches generating a template for the displaying representing an ideal modulated signal (Fig.3 and column 5 lines 12-38, where the small circles located on the circle 311, 315, 312, and 313 are the ideal modulation signal and the star 303 represents the received signal) in order to provide the constant modulus (CM) criterion to the system for easy calculating the dispersion constant so applying a CM criterion to the constellation does not penalize spatial rotation of the constellation due to residual carrier offset.

Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include means for generating a template for the displaying means representing an ideal modulated signal as taught by Touzni et al. into the modified conventional receiver as described by the admitted prior art of the instant application (page 11 lines 1-16) and Takao et al. so as to provide the constant modulus (CM) criterion to the system for easy calculating the dispersion constant so applying a CM criterion to the constellation does not penalize spatial rotation of the constellation due to residual carrier offset.

(10) Response to Argument

Claim Rejections under 35 USC§ 103(a)

Claims 2 and 3

1. Applicant's argument – "In the Final Rejection dated July 29, 2009, the Examiner rejected claims 2 and 9 under 35 U.S.C. § 103(a) as being unpatentable over Takao et al. (U.S. Patent No. 5,920,220) ("Takao") in view of the admitted prior art of the present application ("the APA"); rejected claims 3 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Takao in view of the APA and further in view of Touzni et al. (U.S. Patent No. 7,031,405) ("Touzni"); objected to claims 4-7 and 11-14 as being dependent upon a rejected base claim, but indicated that they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In the Advisory Action dated August 27, 2009, the Examiner maintained the rejection against claims 9 and 10, but indicated that claims 2 and 3 were allowed without explanation, as well as claims 4-7 which depend from them.

Appellant is confused as to why the Examiner would maintain the rejection against claims 9 and 10 while allowing claims 2 and 3, because claims 9 and 10 are essentially equivalent to claims 2 and 3 but in a different form (claims 9 and 10 are in method form whereas claims 2 and 3 are in means-plus-function form), and in the Final Rejection the Examiner had only rejected these claims under 35 U.S.C. § 103(a), which is not a subject-matter-based rejection. For this reason

and other reasons discussed below, Appellant is not entirely certain what the Status of the Claims is. Erring on the side of caution, Appellant will present arguments below in response to every rejection given in the Final Rejection." as recited in pages 11-12 of the Appeal Brief, dated 12/10/2009.

Examiner's Response –

- A. As indicated in Advisory action, dated 8/27/2009, Examiner withdrawn claims 2 and 3 rejections with respect to 35 USC 112 6th paragraph.
- B. Examiner maintains the claims 9 and 10 rejections since they are method claims that are traded differently from the means plus function (35 USC 112 6th paragraph) claims 2 and 3.

Claims 2 and 9, independent claims

1. Applicant's argument – The detailed Applicant's argument is in pages 12-16 of the Appeal Brief. However, it can be summarized as followings –

1.1. Appellant respectfully asserts that the Examiner's interpretation of Takao is improper because the Examiner uses Takao's A/D converters 2 and 3 to describe both Appellant's "means for deriving.., a symbol clock... " and "means for sampling the quadrature component signals ..." (underlined above). However, Takao's A/D converters 2 and 3 cannot be used to satisfy both claim limitations.

1.2. The Examiner construes the claim limitation "means for sampling the quadrature component signals with the sample clock to produce pseudo-symbols..." to be superfluous and redundant as follows: First, the Examiner asserts that Takao describes "means for deriving.., a symbol clock from the

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modulated signal" where Takao generates the signal t0 from the IF input signal "via elements 1, 2, 3, 123, 124, 32f, and 7." (Final Rejection, page 3) Note that during the process of generating t0 from the IF input signal, A/D converters 2 and 3 must sample the output signals of the quadrature detector 1 to generate the I and Q signals. Then, the Examiner asserts that Takao describes "means for sampling the quadrature component signals with the sample clock to produce pseudo-symbols..." where A/D converters 2 and 3 sample the outputs of the quadrature detector 1 to generate the I and Q signals. However, recall that the A/D converters 2 and 3 *already* sampled the output signals of the quadrature detector 1 in order to generate the I and Q signals in the "means for deriving..., a symbol clock from the modulated signal." Thus, the Examiner's construction of claims 2 and 9 unreasonably renders the claim limitation "means for sampling the quadrature component signals with the sample clock to produce pseudo-symbols..." to be superfluous and redundant.

Examiner's Response –

A. Examiner withdraws the claim 2 rejection and maintains claim 9 rejection as addressed in the above paragraph. The detailed Examiner response regarding to claim 9 rejection is shown as below.

B. Examiner cites the Fig.35 of Takao's reference to indicate the equivalence elements with respect to the Fig.15 of the instant application that comprising the claim 9 limitation.

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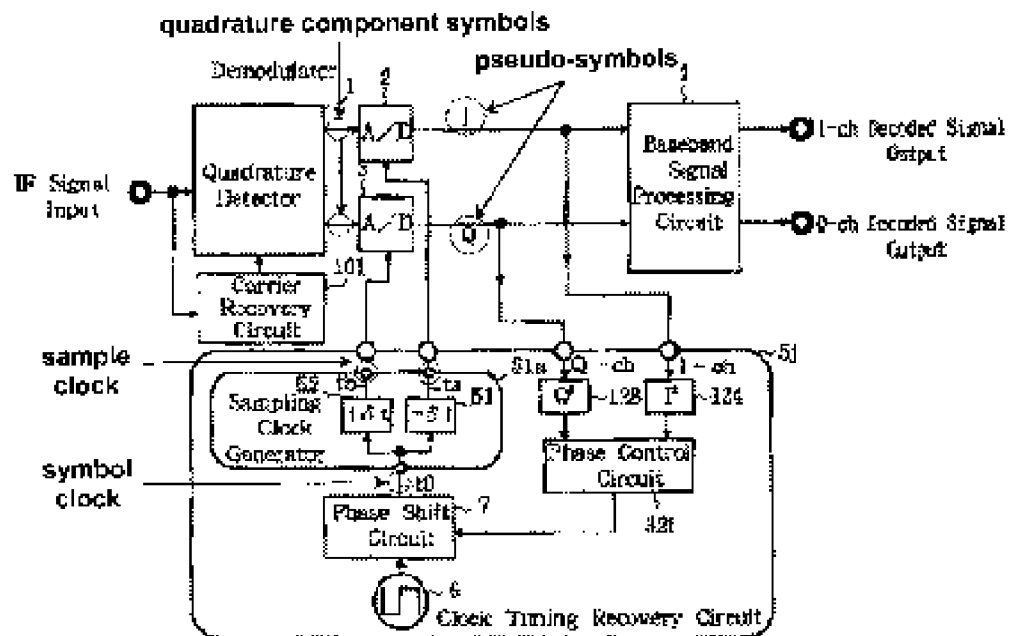


FIG.35 of Takao's reference (US 5,9202,20)

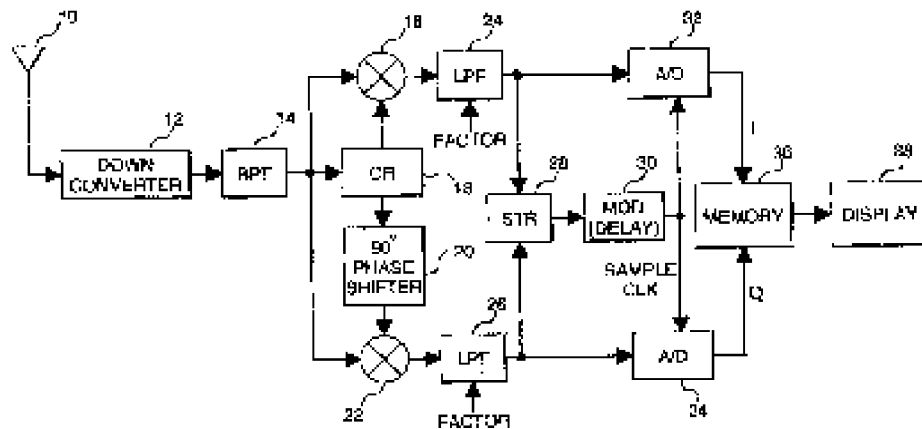


FIG.15 of the Instant Application

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The followings are the one to one element mapping (or equivalence) for Fig.35 of Takao's reference to the Fig.15 of the instant application comprising claim 2 limitation.

Fig.35 of Takao's reference	Fig.15 of Instant Application	Remark
IF signal Input	BPF 14 output signal	It is inherent that the BPF 14 output signal is an IF signal since it is a filtered IF signal been downconverted by the down converter 12.
Demodulator - Quadrature detector 1 and Carrier Recovery Circuit 101	Demodulator – Demodulator 16 and 22, Carrier Recover (CR) 18 and 90° Phase Shifter 20	Since the demodulator of Takao is a quadrature demodulator (generating I and Q signals), it is inherent that the 90° Phase Shifter is included in the quadrature detector 1.
Clock Timing Recovery Circuit 5j excludes Sampling Clock Generator 31a	Symbol Timing Recovery (STR) 28	1. The Clock Timing Recovery Circuit 5j receives <u>digital I & Q signals (after A/D)</u> to derive the symbol clock. 2. The Symbol Timing Recovery (STR) 28 receives

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		analog I & Q signals (before A/D) to derive the symbol clock
Sampling Clock Generator 31a	MOD (Delay) 30	The Sampling Clock Generator 31a delays symbol clock t_0 by δt (elements 51 and 52)
A/D 2, 3	A/D 32, 34	

Based on the comparison table shown above, we can conclude that Fig.35 of Takao's reference has the same structure as that of Fig.15 of the instant application except for the followings –

1. The Clock Timing Recovery Circuit 5j receives **digital I & Q signals (after A/D)** to derive the symbol clock. Instead, the Symbol Timing Recovery (STR) 28 of instant application receives analog I & Q signals (before A/D) to derive the symbol clock.

That is, the location of A/D 2, 3 and the Clock Timing Recovery Circuit 5j (including Sampling Clock Generator 31a) of Takao's is switched by the instant application (Fig.15 elements A/D 32, 34, and STR 28 and MOD (DEALY) 30). It would have been obvious to one having ordinary skill in the art at the time the Invention was made to have element 5j of Fig.35 of Takao to receives analog I and Q signals before A/D 2 & 3 to derive the symbol clock, since it has been held

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that rearranging parts of an- invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

C. In response to Applicant's arguments 1.1 & 1.2

As addressed in the above paragraph, the Clock Timing Recovery Circuit 5j receives digital I & Q signals I & Q (after A/D) to derive the synchronized symbol clock (t_0) with respect to the IF signal input (Fig.35, it is inherent that this IF signal is derived from a modulated signal transmitted by a transmitter). Then, delays the symbol clock by the sampling Clock Generator 31a to generate the synchronized sampling clock t_a , t_b for sampling A/D.

Before the squaring circuits 123 & 124 and Phase Control Circuit 32f take place, the symbol clock t_0 is the fixed clock provide by the system clock generator 6 that is not synchronized with input signal and the sampling clock t_a & t_b are generated from the unsynchronized symbol clock t_0 . At this time instance, the A/D 2 & 3 are sampled by the unsynchronized sampling clock t_a & t_b .

After the squaring circuits 123 & 124 and Phase Control Circuit 32f take place, the squaring circuits 123 & 124 square the unsynchronized digital I and Q samples and input to the phase control circuit 32f (Fig.36 and col. 25 lines 36-49) to generate a correction signal to the phase shift circuit 7 (Fig.9 and col.12 line 66 and col.13 line 49) to generate the synchronized symbol clock t_0 . The synchronized symbol clock t_0 is inputted to the sampling clock generator 31a to generate the synchronized or corrected sampling clock t_a & t_b . The A/D 2 & 3 are

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sampled by the synchronized or corrected sampling clock t_a & t_b to convert the analog I & Q signal to digital form.

The Fig.30a - Fig.30g can be used to illustrate the clock relationship among system clock 6 (Fig.30d), symbol clock t_0 (Fig.30f), and sampling clock t_a (Fig.30f) and t_b (Fig.30g).

The clock timing recovery circuit 5j is simply a feedback time recovery loop used to recover the symbol clock from the input signal (IF signal, Fig.35). The only function for A/D converters 2 & 3 here is to convert the demodulated analog I & Q signals to digital form with sampling clock t_a & t_b .

As described in the above paragraph the Fig.35 of Takao's reference has the same structure as that of Fig.15 of the instant application except for the followings –

1. The Clock Timing Recovery Circuit 5j receives **digital I & Q signals (after A/D)** to derive the symbol clock. Instead, the Symbol Timing Recovery (STR) 28 of instant application receives analog I & Q signals (before A/D) to derive the symbol clock.

Furthermore, the claim limitation does not limit “deriving a symbol clock and sampling the quadrature component signal ...” to be two unrelated circuits without feedback loop.

Thus, it is concluded that Takao's reference teaches a receiver that appears to be an obvious variant of the receiver disclosed in the instant application. It is inherent that Takao's receiver will perform the same function as

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that of the instant application. Under the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986).

Claims 3 and 10, dependent claims

1. Applicant's argument – “Claims 3 and 10 are allowable because they depend from claims 2 and 9 respectively, both of which are allowable for the reasons discussed above. Furthermore, the addition of Touzni does not remedy any of the deficiencies of the Examiner's proposed combination regarding claims 2 and 9 discussed above. For these reasons, claims 3 and 10 are not rendered obvious by Takao in view of the APA and further in view of Touzni. Accordingly, Appellant requests that the rejection of claims 3 and 10 under 35 U.S.C. § 103(a) be reversed.” as recited in page 16 of the Appeal brief, dated 12/10/2009.

Examiner's Response –

A. Examiner withdraws the claim 3 rejection and maintains the claim 10 rejection as explained in the above paragraph. The Examiner Response with respect to claim 10 rejection has been addressed in the above paragraph.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Ted Wang, Ph.D

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